REMARKS

I. Introduction

In response to the office action dated March 14, 2006, Applicants have amended claim 13 to more particularly point out and distinctly claim the subject matter of the invention. Claims 14 and 15 have been canceled. In addition, the title of the invention has been amended. No new matter has been added.

As a preliminary matter, please note that original claims 27 – 30 were not examined in the office action dated March 14, 2006. The Examiner was informed of this error by telephone and acknowledged the mistake. Accordingly, if the Examiner intends to reject claims 27 – 30 in a future office action, this rejection cannot be made final because claims 27 – 30 were never examined.

Additionally, the Examiner has indicated that the data provided by Applicants regarding PCT is not consistent with PTO records. Applicants respectfully request that the Examiner provide additional information regarding what is inconsistent so as to allow the Applicants to address the Examiner's concerns.

In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Claim Rejections Under 35 U.S.C. § 103

Claims 13 – 15 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,280,192 to Kryzaniwsky in view of U.S. Patent No. 5,259,110 to Bross. Applicants traverse this rejection for at least the following reasons.

The present invention relates to a method of forming a module component which includes the step of forming a plurality of penetration holes according to a predetermined matrix

of N aligned rows and M aligned columns, where each of the penetration holes is aligned in both a row and a column, each row and column has at least three penetration holes, and there are at least three rows and three columns in the matrix. By providing such a matrix of penetration holes, chip components can be automatically inserted into the penetration holes by a machine in an efficient manner. As a result, performance of the inserting machine is enhanced, thereby realizing size-reduction of the chip components and pitch narrowing of the penetration holes.

For example, as shown in Fig. 3(a) of Applicants' drawings, the plurality of penetration holes form a NxM matrix, or in this instance, a 6-by-6 matrix of aligned rows and aligned columns. Each of the penetrations holes is formed precisely at a location or position according to the predetermined matrix of rows and columns. Thereafter, a specific number of chip components are inserted at the positions or locations of these penetration holes. By inserting chip components into these penetration holes formed in accordance with the predetermined matrix, the performance of the automatic chip-inserting machine can be enhanced (*see*, e.g., page 5-6 of specification).

Turning to the prior art, Kryzaniwsky merely discloses forming a plurality of chip wells 28-33 in dielectric layer 11 so as to allow for placement of chips 5-10. However, Kryzaniwsky does not disclose forming an NxM matrix of penetration holes, which extend through the substrate. Indeed, as shown in Figs. 1C and 1D of Kryzaniwsky, the wells 28-33 are formed by removing some of the dielectric layer 11 previously deposited on plate 1. There is no forming of penetration holes extending through the substrate as taught by the present invention. Thus, at a minimum, Kryzaniwsky fails to disclose or suggest the recited step of forming the penetration holes in a matrix of N aligned rows and M aligned columns.

Bross also fails to disclose forming a plurality of penetration holes in a matrix of N aligned rows and M aligned columns, where each of the penetration holes is aligned in both a row and a column, each row and column has at least three penetration holes, and there are at least three rows and three columns in the matrix.

Thus, even assuming *arguendo* that the combination of Kryzaniwsky and Bross is proper, at a minimum, the combination still fails to disclose or suggest the step of forming the penetration hole matrix as recited by the pending claims. Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (MPEP § 2143.03), and the combination of the Kryzaniwsky and Bross fails to do so, it is respectfully submitting that claim 13 is patentable over the cited references taken alone or in combination with one another.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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